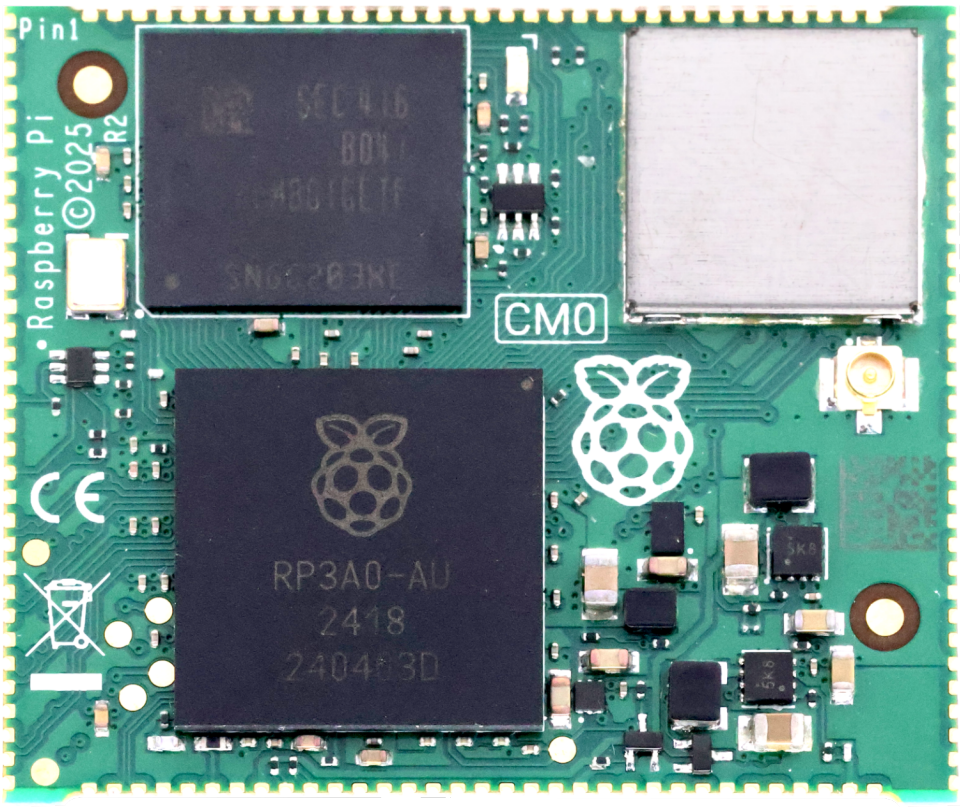


# Raspberry Pi Compute Module Zero

## Data Sheet

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# Raspberry Pi Compute Module Zero

## Documentation Description

The Raspberry Pi Compute Module Zero is an official Raspberry Pi product. The product brand belongs to Raspberry Pi, and the product IP belongs to Raspberry Pi.

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The final interpretation and most accurate documentation version shall be based on the official content released by Raspberry Pi.

# 1 Introduction

This section introduces the definition and features of the Raspberry Pi Compute Module Zero (CM0).

## 1.1 Overview

The CM0 is a System-on-Module (SoM) built around the RP3A0 chip, which is developed in-house by Raspberry Pi and utilizes a customized system-level packaging design. The CM0 module integrates onboard RAM and optional wireless networking capabilities within a compact, embeddable form factor, fully realizing the core processing power of the Raspberry Pi Zero 2 W. This enables developers and system designers to integrate Raspberry Pi functionality into customized hardware designs.

The Raspberry Pi CM0 module employs a direct solder-to-carrier board design, achieving electrical connectivity through 132 pins distributed along the module's edge. These pins are arranged in a 1mm pitch grid. The module supports both manual soldering and automated PCB assembly using standard surface mount technology (SMT) processes.

Since the CM0 module is developed based on the Raspberry Pi Zero 2 W architecture, developers can test their projects on the Raspberry Pi Zero 2 W platform before building the final CM0 product. As a new core module, CM0 targets the entry-level segment of the existing market, achieving breakthroughs through a combination of low cost and high performance. For cost-sensitive applications, a simplified version without eMMC flash memory is available, designated as CM0 Lite.

> Note
>
> Unless otherwise specified, references to CM0 in this document also include CM0Lite.

Figure 1 CM0

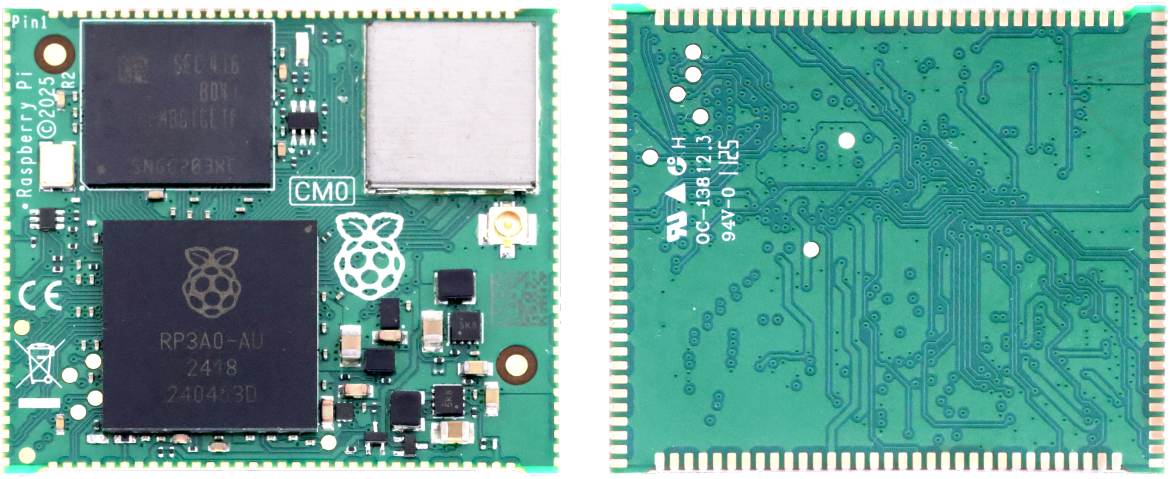
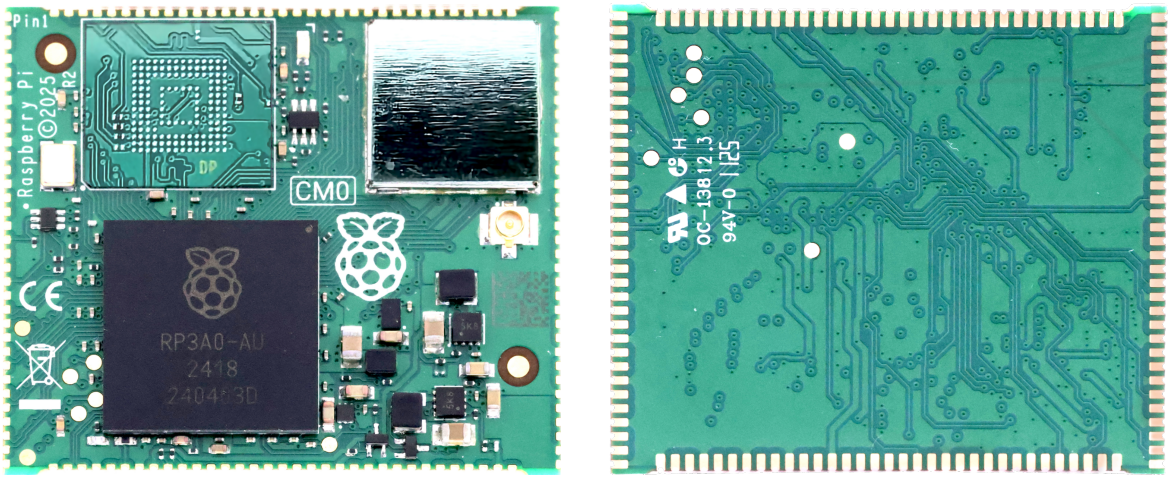



Figure 2 CM0Lite




## 1.2 Features

The primary features of CM0 are as follows:

- High-performance SoC: Broadcom BCM2837, 1GHz quad-core 64-bit Arm Cortex-A53 processor
- Compact Package: 39mm × 33mm × 2.8mm module
- Pinout: 132-pin layout with 1mm pitch
- Video Support: Full HD (1080p) 30fps video encoding/decoding
  - Supports H.264/MPEG-4 format 1080p30 decoding
  - Supports H.264 1080p30 encoding
- Graphics Support: 2D/3D graphics processing via OpenGL ES 1.1/2.0
- Memory Configuration: 512MB LPDDR2 RAM
- Optional Storage: On-board 8GB or 16GB eMMC flash
- Additional SDIO interface (CM0Lite only): Enables external storage or peripheral expansion as an alternative to onboard eMMC
- Wireless connectivity (optional): Supports Wi-Fi and Bluetooth (with IPEX-1 external antenna connector)
- 1 x USB 2.0 port
- 28-channel GPIO (General-Purpose Input/Output)
- Camera Support: 4-channel CSI camera interface
- Video Output:
  - 1 x HDMI port, supporting 1080p at 30Hz
  - 1 x 4-channel MIPI DSI display port
  - 1 x DPI display interface

    - 1 x Composite video port
- Single +5V power input
- On-board green LED status indicator

# 2 Interfaces

CM0 provides diverse interface support to meet various application needs, ranging from data storage and network communication to wireless connectivity, display output, and flexible GPIO expansion. These interfaces enable developers to build embedded systems with connectivity and high adaptability. Technical specifications for each interface, including configuration options, wiring guidelines, and design considerations, are provided below.

## 2.1 Wireless

CM0 supports Wi-Fi and Bluetooth functionality, allowing developers and system designers to flexibly manage wireless connectivity for diverse applications. Its wireless interface is provided by the Cypress CYW43439 chip, specifically supporting:

- 2.4 GHz IEEE 802.11 b/g/n Wi-Fi
- Bluetooth 5.0 and Bluetooth Low Energy (BLE)

> Note
>
> The Bluetooth version for CM0 units in initial small-batch trial production is Bluetooth 4.2. The Bluetooth version for CM0 units in later mass production will be Bluetooth 5.0

The antenna uses a standard IPEX-1 interface. Raspberry Pi Ltd provides certified compatible antennas. If you choose a third-party antenna, you must obtain certification yourself. Raspberry Pi does not provide certification support for unauthorized antennas.

Users can independently enable or disable wireless functionality as needed. For example, in self-service kiosk scenarios, service engineers may temporarily activate wireless for system updates and subsequently disable it to meet security and regulatory compliance requirements.

To support power optimization and regulatory compliance, the CM0 reserves two control pins: `WiFi_ON` and `BT_ON`

> Note
>
> On CM0 modules without Wi-Fi functionality, the `WiFi_ON` and `BT_ON` pins are reserved.

### 2.1.1 WiFi_ON

The WiFi_ON pin indicates the enabled/disabled status of Wi-Fi and can be used to disable Wi-Fi. This pin can only be pulled low and cannot be driven high; when required, the software driver internally pulls it high.

- If this pin is high (logic 1), Wi-Fi is enabled. If Wi-Fi is re-enabled after being disabled, the Wi-Fi driver must be reinitialized.
- Driving or pulling this pin low (logic 0) prevents Wi-Fi from being enabled, aiding in power reduction or meeting requirements for physically disabling Wi-Fi.

### 2.1.2 BT_ON

The BT_ON pin indicates the enabled/disabled state of Bluetooth and can be used to disable Bluetooth. This pin can only be pulled low and cannot be driven high; the software driver internally pulls it high when required.

- If this pin is high (logic 1), Bluetooth is enabled. If Bluetooth is re-enabled after being disabled, the Bluetooth driver must be reinitialized.
- Driving or pulling this pin low (logic 0) prevents Bluetooth from being enabled, aiding in power saving or meeting physical disabling requirements.

## 2.2 USB 2.0

The USB 2.0 interface supports a maximum signal transfer rate of 480 Mb/s. Differential pairs should be routed with a 90Ω differential impedance. The P and N signals within each differential pair should be length-matched, with an ideal tolerance of 0.15mm or less.

To enable USB 2.0 functionality, set the following in config.txt. Add `config.txt` `dtoverlay=dwc2,dr_mode=host` to set

> Note
>
> USB 2.0 port support for USB OTG mode operation. Although this feature is not explicitly documented in official materials, users have successfully enabled it. The `USB_OTG_ID` pin determines the device role (host or slave) and typically connects to the ID pin of the Micro USB interface. To use OTG functionality, enable it in the operating system (OS). To fix the device role, ground the `USB_OTG_ID` pin.

## 2.3 CSI (MIPI camera)

The CM0 module supports a 4-channel CSI interface for high-speed camera connectivity. This interface employs four sets of 100Ω differential signal pairs, with wire length mismatch within the same differential pair requiring control within 0.15mm.

The Raspberry Pi official firmware supports the following camera sensors:

- OmniVision OV5647
- Sony IMX219
- Sony IMX296
- Sony IMX477
- Sony IMX708

For detailed information about the CSI interface, please refer to the official Raspberry Pi technical documentation (https://www.raspberrypi.com/ documentation/accessories/camera.html).

## 2.4 Video and Display Interfaces

The CM0 module supports multiple display interfaces (as shown in Table 1) and can drive up to three displays simultaneously (supporting any combination of the following interface types).

Table 1 Video and Display Interfaces for CM0

| Interface Type | Description |
| --- | --- |
| HDMI | High-speed digital differential signal display interface; 1080p30 (Full HD 30 frames) |
| DSI | High-speed 4-channel differential pair display interface |
| DPI | Parallel Display Interface via GPIO |
| CVBS | Analog composite video interface; requires 75Ω termination impedance matching |

### 2.4.1 HDMI

The CM0 module supports one HDMI output port capable of 1080p30 resolution. To ensure stable HDMI operation, observe the following design considerations:

- HDMI signals must be routed as 100Ω differential pairs;
  - Signal length mismatch within the same differential pair should be controlled within 0.15mm;
  - Length mismatch between different differential pairs must be controlled within 25mm.
- Supports Consumer Electronics Control (CEC) functionality with an integrated 27kΩ pull-up resistor within the CM0;
- Supports Hot Plug Detection (HPD) functionality, with a 100kΩ pull-down resistor integrated internally in the CM0;
- Integrated pull-up resistor for Extended Display Identification Data (EDID) signal within CM0;
- Like the Pi5, the CM0 does not incorporate additional ESD protection on the HDMI signal lines (typically not required). Evaluate whether external ESD protection circuitry is necessary based on your specific application.

### 2.4.2 DSI

The CM0 module supports connecting DSI-compatible displays via a high-speed digital DSI interface. This interface uses four differential signal pairs and must be routed with 100Ω differential impedance. Signal length mismatch within the same differential pair should be controlled within 0.15mm.

The CM0 is compatible with displays supported by the following systems:

- Raspberry Pi Official Firmware
- Mainline Linux kernel

For third-party displays not officially supported, custom drivers must be provided.

### 2.4.3 DPI

The CM0 module supports up to 24-bit RGB video output with four control signals: Pixel Clock (PCLK), Data Enable (DE), Vertical Sync (VSYNC), and Horizontal Sync (HSYNC). This Display Parallel Interface (DPI) utilizes GPIO pin resources.

Some GPIO functionality can be preserved by configuring a lower color depth.

### 2.4.4 CVBS

The CM0 module supports standard analog video output in multiple formats (composite video, also known as CVBS). The CVBS signal is designed to drive a 75Ω impedance mode.

## 2.5 I2C Interface

The CM0 module provides two reconfigurable I2C buses whose functions can be adjusted based on system configuration and peripheral usage.

### 2.5.1 CSI/DSI I2C Bus (SDA0 and SCL0)

These I2C buses are assigned by default to the CSI and DSI interfaces. However, when the CSI/DSI interfaces are disabled, they can be reconfigured for general-purpose I2C bus or GPIO functionality:

- Serial data pin (SDA0) connects to GPIO44.
- The serial clock pin (SCL0) connects to GPIO45.

### 2.5.2 HAT Expansion Board EEPROM Identifies I2C Bus (ID_SD and ID_SC)

The HAT expansion board EEPROM identifies the I2C bus through the ID_SD (data) and ID_SC (clock) pin signals. This bus is typically dedicated for HAT expansion board identification.

If the firmware does not utilize this I2C bus (e.g., when no HAT ID EEPROM is connected), these pins can be reconfigured as GPIO0 and GPIO1 functionality. When these pins are required for GPIO use, add the following to the `config.txt` file:

```
force_eeprom_read=0
```

This setting prevents the firmware from detecting the HAT EEPROM.

## 2.6 SDIO (CM0Lite only)

The CM0Lite version does not feature onboard eMMC storage but provides a Secure Digital Input/Output (SDIO) interface for connecting external storage devices. To ensure stable signal transmission, the SDIO interface requires configuration with a reference voltage (SD_VREF) corresponding to the storage type in use. The SDIO storage configuration for CM0Lite is detailed in Table 2 below:

Table 2 SDIO Storage Configuration

| Storage Type | Connection | Reference Voltage |
|---|---|---|
| External eMMC | SDIO | Connect SD_VREF to the 1.8V power supply (CM0_1.8V pin) to enable 1.8V signal transmission |
| External SD Card | SDIO | Connect SD_VREF to the 3.3V power supply (CM0_3.3V pin) to enable 3.3V signal transmission |
| On-board eMMC | SDIO | No connection required; SD_VREF pin may be left floating or connected to 1.8V power supply (CM0_1.8V pin) |

## 2.7 GPIO

Provides 28 general-purpose input/output (GPIO) pins, corresponding to the GPIO pins on the Pi5's 40-pin connector. These pins provide access to internal peripherals such as SMI, DPI, I2C, PWM, SPI, and UART. Detailed information on related functionalities and multiplexing options aligns with the BCM2835 ARM Peripherals documentation (https://www.raspberrypi.org/app/uploads/2012/02/BCM2835-ARM-Peripherals.pdf).

To minimize electromagnetic compatibility (EMC) issues, it is recommended to set drive strength and slew rate to the minimum levels required.

GPIO2 and GPIO3 incorporate built-in 1.8kΩ pull-up resistors.

The power supply for the GPIO group is provided by the GPIO_VREF power pin. This pin can be connected to CM0_1.8V for 1.8V signal levels or to CM0_3.3V for 3.3V signal levels. The total current load across all 28 GPIO pins must not exceed 50mA. GPIO_VREF must be connected to either the CM0_3.3V or CM0_1.8V power supply.

### 2.7.1 Multifunction Assignment

GPIO pins support up to six multiplexed function assignments. Table 3 provides an overview of these multiplexed functions; detailed descriptions are available in the Peripheral Data Manual (https://www.raspberrypi.com/documentation/computers/processors.html#bcm2837).

Only one function may be enabled for each GPIO at a time. Unnamed function options in Table 3 are reserved functions. Table 3 GPIO Function Selection

| GPIO | Default Pull | Function | | | | | |
|---|---|---|---|---|---|---|---|
| | | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 |
| 0 | High | SDA0 | SA5 | DPI_PCLK | | | |
| 1 | High | SCL0 | SA4 | DPI_DE | | | |
| 2 | High | SDA1 | SA3 | DPI_VSYNC | | | |
| 3 | High | SCL1 | SA2 | DPI_HSYNC | | | |
| 4 | High | GPCLK0 | SA1 | DPI_D0 | | | ARM_TDI |
| 5 | High | GPCLK1 | SA0 | DPI_D1 | | | ARM_TDO |
| 6 | High | GPCLK2 | SOE_N | DPI_D2 | | | ARM_RTCK |
| 7 | High | SPI0_CSn1 | SWE_N | DPI_D3 | | | |
| 8 | High | SPI0_CSn0 | SD0 | DPI_D4 | | | |
| 9 | Low | SPI0_MISO | SD1 | DPI_D5 | | | |
| 10 | Low | SPI0_MOSI | SD2 | DPI_D6 | | | |
| 11 | Low | SPI0_SCLK | SD3 | DPI_D7 | | | |
| 12 | Low | PWM0 | SD4 | DPI_D8 | | | ARM_TMS |
| 13 | Low | PWM1 | SD5 | DPI_D9 | | | ARM_TCK |
| 14 | Low | TXD0 | SD6 | DPI_D10 | | | TXD1 |
| 15 | Low | RXD0 | SD7 | DPI_D11 | | | RXD1 |
| 16 | Low | FL0 | SD8 | DPI_D12 | CTS0 | SPI1_CSn2 | CTS1 |
| 17 | Low | FL1 | SD9 | DPI_D13 | RTS0 | SPI1_CSn1 | RTS1 |
| 18 | Low | PCM_CLK | SD10 | DPI_D14 | | SPI1_CSn0 | PWM0 |
| 19 | Low | PCM_FS | SD11 | DPI_D15 | | SPI1_MISO | PWM1 |
| GPIO | Default Pull | Function | | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 20 | Low | PCM_DIN | SD12 | DPI_D16 | | SPI1_MOSI | GPCLK0 |
| 21 | Low | PCM_DOUT | SD13 | DPI_D17 | | SPI1_SCLK | GPCLK1 |
| 22 | Low | SD0_CLK | SD14 | DPI_D18 | SD1_CLK | ARM_TRST | |
| 23 | Low | SD0_CMD | SD15 | DPI_D19 | SD1_CMD | ARM_RTCK | |
| 24 | Low | SD0_DAT0 | SD16 | DPI_D20 | SD1_DAT0 | ARM_TDO | |
| 25 | Low | SD0_DAT1 | SD17 | DPI_D21 | SD1_DAT1 | ARM_TCK | |
| 26 | Low | SD0_DAT2 | TE0 | DPI_D22 | SD1_DAT2 | ARM_TDI | |
| 27 | Low | SD0_DAT3 | TE1 | DPI_D23 | SD1_DAT3 | ARM_TMS | |
| 28 | None | SDA0 | SA5 | PCM_CLK | FL0 | | |
| 29 | None | SCL0 | SA4 | PCM_FS | FL1 | | |
| 40 | Low | PWM0 | SD4 | | SD1_DAT4 | SPI2_MSIO | TXD1 |
| 41 | Low | PWM1 | SD5 | TE0 | SD1_DAT5 | SPI2_MOSI | RXD1 |
| 42 | Low | GPCLK0 | SD6 | TE1 | SD1_DAT6 | SPI2_SCLK | RTS1 |
| 44 | None | GPCLK1 | SDA0 | SDA1 | TE0 | SPI2_CSn1 | |
| 45 | None | PWM1 | SCL0 | SCL1 | TE1 | SPI2_CSn2 | |

### 2.7.2 GPIO Multifunction

Multiple GPIO multiplexing functions support various peripheral interfaces and communication protocols. The following list summarizes available peripherals and their supported configurations:

- 2 UART interfaces, including standard signals (Transmit TXD, Receive RXD, Clear to Send CTS, Ready to Send RTS)
- 1 4-bit SDIO interface
- 2 Pulse Width Modulation (PWM) channels
- 3 General-Purpose Clock (GPCLK) outputs
- 1 Display Parallel Interface (DPI) with pixel clock PCLK, data enable DE, vertical sync VSYNC, horizontal sync HSYNC, and up to 24-bit data bus
- 2 I2C controllers
- 3 SPI controllers

### 2.7.3 Camera GPIO (CAM_GPIO)

The CM0 module provides a dedicated GPIO pin for controlling the camera module, designated as CAM_GPIO0. This control signal is typically connected to pin 17 of the camera interface to manage the camera module's power supply. CAM_GPIO0 corresponds to the on-board GPIO40 pin.

## 2.8 Status LED (LED_nACT)

The GPIO29 pin on the SoC controls the LED_nACT signal, which replicates the LED used to display the board's operational status. This status LED behaves similarly to the green LED feature on the Raspberry Pi Zero 2 W. On Linux systems:

- The LED flashes when data is being read from or written to the eMMC or SD card.
- If an error occurs during boot, the LED flashes according to specific error code patterns.

Refer to the https://www.raspberrypi.com/'s official documentation for LED flash codes (https://www.raspberrypi.com/documentation/computers/configuration.html#led-warning-flash-codes) to interpret specific error code patterns.

This signal is active low. A signal buffer must be added if driving an external LED is required.

## 2.9 Power Management and Control

The signals listed in Table 4 pertain to CM0's power sequencing control, boot source selection, and system readiness indication:

Global Enable signal

(GLOBAL_EN), Raspberry Pi boot mode selection (nRPI_BOOT), and run power good indication

(RUN_PG).

Table 4 System Control Signals

| Pin | Description | Use |
|---|---|---|
| GLOBAL_EN | Controls the power-down state of the CM0 module | Pulling this pin low enables CM0 to enter its lowest power state. It is recommended to pull this pin low only after the operating system (OS) has completed shutdown operations. |
| nRPI_BOOT | Determines the boot source during startup | Maintaining a low level during boot bypasses eMMC and boots via the USB 2.0 interface. |
| RUN_PG | This signal goes high when the power supply unit (PSU) completes power-up. | This signal may be actively pulled low to delay power-up or reset the module. It is recommended to pull this pin low only after the operating system (OS) has completed shutdown operations. |

# 3 Power

The CM0 module requires a regulated 5V DC supply for proper operation. It also provides 3.3V and 1.8V voltage outputs (up to 600mA current) for external devices. The following sections detail the required power-up/power-down sequencing, typical and maximum power consumption values, and parameters for the onboard voltage regulators.

## 3.1 Power-Up Sequence

The following list summarizes the power-up conditions and timing requirements for normal CM0 startup:

- No pins may be powered before the 5V power rail is activated.
- To boot CM0 via USB, the nRPI_BOOT pin must remain low for 1ms after the 5V power rail rises.
- The 5V power rail should rise monotonically to at least 4.75V and remain above this voltage during operation.
- Power-up sequencing begins after the 5V power rail exceeds 4.75V and the GLOBAL_EN signal transitions high.
- Power and signals are activated in the following sequence:
  1. The 5V power rail rises.
  2. GLOBAL_EN signal rises.

3. The CM0_3.3V power rail rises.
4. The CM0_1.8V power rail rises (delayed by at least 1ms after the CM0_3.3V rise).

## 3.2 Power-Down Sequence

The following list summarizes CM0's recommended power-down procedures and precautions to ensure safe shutdown and file system integrity:

- To guarantee file system consistency, shut down the operating system before powering off.
- If a controlled shutdown cannot be achieved, it is recommended to use `btrfs`、`f2fs` or `overlayfs` etc. (accessible via `raspi-config` tool).
- After the operating system completes shutdown, the 5V power rail can be disconnected or the `GLOBAL_EN` pin pulled low to enter CM0's `CM0_1.8V` r mode.
- During power-down, power rails discharge before the `CM0_3.3V` power rail.

## 3.3 The power supply rail

The actual power consumption of CM0 depends on the type of task being executed, with typical values as follows:

- The lowest shutdown power consumption occurs when `GLOBAL_EN` when the pin is pulled low, with a typical value of approximately 500μA.
- Typical idle power consumption is 225mA (actual value varies by operating system).
- Typical operating power consumption is approximately 675mA (depending on the operating system and running tasks).

## 3.4 Regulator Outputs

CM0 incorporates voltage regulators that provide 3.3V (CM0_3.3V) and 1.8V (CM0_1.8V) power rails. Each regulator can supply up to 600mA to external devices connected to the board.

> Note
>
> Current drawn by peripherals from these regulators is not included in the total power consumption data. The specified power consumption values only include the board's own power consumption and do not include the power consumption of peripherals powered by the regulators.

# 4 Specifications

This section provides technical specifications for the CM0 module components, including dimensional specifications, pin definitions, electrical parameters, thermal characteristics, and Mean Time Between Failures (MTBF) calculations.

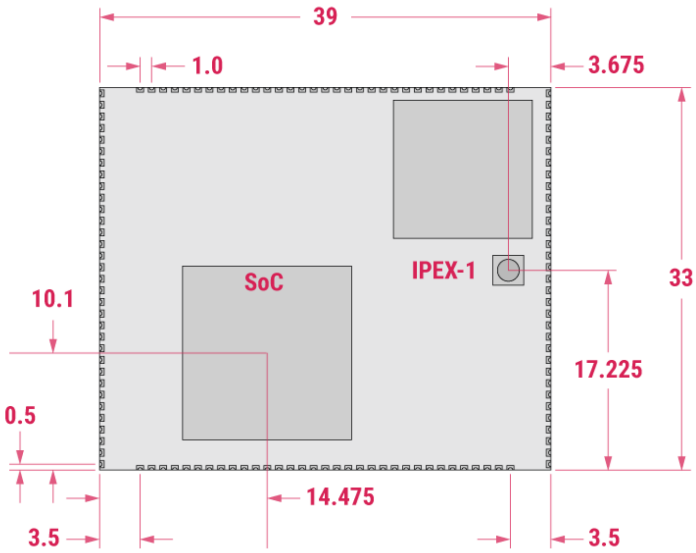
## 4.1 Mechanical Specifications

The CM0 utilizes a compact PCB board constructed from FR4 material. Its 132 pins feature 1mm pitch pads, employing a semi-plated through-hole process with high-quality electroless nickel immersion gold (ENIG) plating to ensure soldering reliability. Subsequent sections will detail the PCB dimensional specifications and recommended package designs.

### 4.1.1 PCB Dimensions

The CM0 is a compact module measuring 39mm × 33mm × 2.8mm. The mechanical schematic in Figure 3 shows a top view of the CM0, including its overall dimensions, external layout of key components (SoC, wireless module, and IPEX-1 connector), and the arrangement of its 132 pins. Pin numbering starts from the upper-left corner of the module and proceeds counterclockwise. Each pin is 0.6mm wide, with 1mm spacing between adjacent pins on the same edge.

Figure 3 CM0 PCB Dimensions



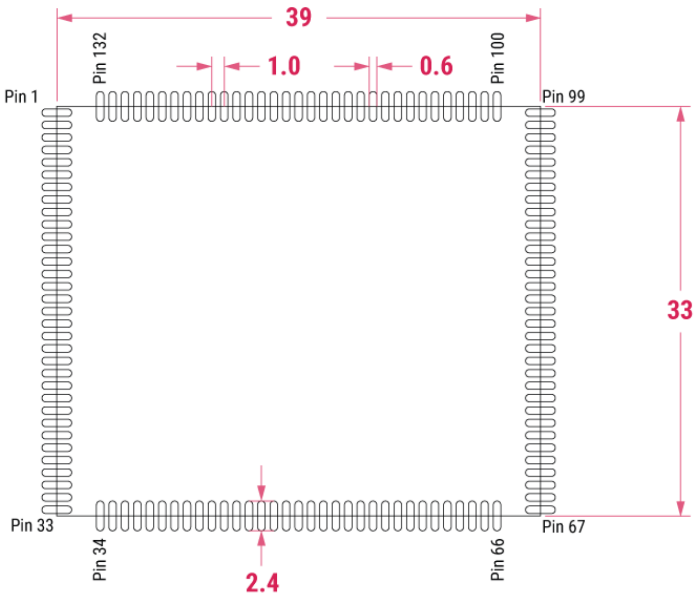

Unit: mm

### 4.1.2 Recommended Package Design

Figure 4 illustrates the recommended

packaging design for CM0. Figure 4

Recommended Packaging Design for CM0




Unit: mm

## 4.2 Pins

The CM0 module contains 132 pins. Specific pin definitions are provided in Table 5. Table 5 CM0 Pin

| Pin | Signal | Description |
|---|---|---|
| 1 | GND | Ground (0V) |
| 2 | DSI_D3_P | Output Display Channel D3 Positive Terminal |
| 3 | DSI_D3_N | Output display channel D3 negative terminal |
| 4 | GND | Ground (0V) |
| 5 | DSI_D2_P | Output Display Channel D2 Positive Terminal |
| 6 | DSI_D2_N | Output display channel D2 negative terminal |
| 7 | GND | Ground (0V) |
| 8 | DSI_CL_P | Output Display Clock Positive |
| 9 | DSI_CK_N | Output Display Clock Negative |
| 10 | GND | Ground (0V) |
| 11 | DSI_D1_P | Output Display Channel D1 Positive Terminal |
| 12 | DSI_D1_N | Output Display Channel D1 Negative Terminal |
| 13 | GND | Ground (0V) |
| 14 | DSI_D0_P | Output Display Channel D0 Positive Terminal |
| 15 | DSI_D0_N | Output display channel D0 negative terminal |
| 16 | GND | Ground (0V) |
| 17 | HDMI_HPD | Input HDMI Hot Plug Detection |
| 18 | HDMI_SDA | Bidirectional HDMI Configuration Data Line (SDA) |
| 19 | HDMI_SCL | Bidirectional HDMI Configuration Clock Line (SCL) |
| 20 | HDMI_CEC | Input HDMI CEC data line (level-shifted to 3.3V LVCMOS via CM0) |
| 21 | GND | Ground (0V) |
| 22 | HDMI_CK_N | Output HDMI clock negative |
| 23 | HDMI_CK_P | Output HDMI clock positive |
| 24 | GND | Ground (0V) |
| 25 | HDMI_D0_N | Output HDMI TX0 Negative |
| Pin | Signal | Description |

| | | |
|---|---|---|
| 26 | HDMI_D0_P | Output HDMI TX0 Positive |
| 27 | GND | Ground (0V) |
| 28 | HDMI_D1_N | Output HDMI TX1 Negative Terminal |
| 29 | HDMI_D1_P | Output HDMI TX1 Positive Terminal |
| 30 | GND | Ground (0V) |
| 31 | HDMI_D2_N | Output HDMI TX2 Negative Terminal |
| 32 | HDMI_D2_P | Output HDMI TX2 Positive Terminal |
| 33 | GND | Ground (0V) |
| 34 | GND | Ground (0V) |
| 35 | USB_N | USB 2.0 D- |
| 36 | USB_P | USB 2.0 D+ |
| 37 | GND | Ground (0V) |
| 38 | USB_OTG | Input (3.3V signal): USB OTG functionality pin; internally integrated pull-up resistor; when this pin is grounded, CM0 switches to USB host mode, but requires proper operating system drivers for operation |
| 39 | CVBS | Composite Video Output |
| 40 | GND | Ground (0V) |
| 41 | CM0_3.3V (Output) | 3.3V ±5% accuracy, maximum output current per pin 300mA, total sum not to exceed 600mA; when GLOBAL_EN is set low, power supply will be cut off |
| 42 | SDA0 | I2C data pin (GPIO44): Typically used for camera and display modules; internally integrated with a 1.8 kΩ pull-up resistor to CM0_3.3V power supply |
| 43 | SCL0 | I2C Clock Pin (GPIO45): Typically used for camera and display modules; internally integrated with a 1.8 kΩ pull-up resistor to CM0_3.3V power supply |
| 44 | CAM_GPIO | 3.3V signal: Can be used as a GPIO (GPIO40) |
| 45 | GND | Ground (0V) |
| 46 | CSI_D3_P | Camera Input D3 Positive Terminal |
| 47 | CSI_D3_N | Camera input D3 negative terminal |
| 48 | GND | Ground (0V) |
| 49 | CSI_D2_P | Camera Input D2 Positive Terminal |
| 50 | CSI_D2_N | Camera Input D2 Negative Terminal |
| 51 | GND | Ground (0V) |
| **Pin** | **Signal** | **Description** |

| | | |
|---|---|---|
| 52 | CSI_CK_P | Camera input clock positive terminal |
| 53 | CSI_CK_N | Camera Input Clock Negative Terminal |
| 54 | GND | Ground (0V) |
| 55 | CSI_D1_P | Camera Input D1 Positive Terminal |
| 56 | CSI_D1_N | Camera Input D1 Negative Terminal |
| 57 | GND | Ground (0V) |
| 58 | CSI_D0_P | Camera Input D0 Positive Terminal |
| 59 | CSI_D0_N | Camera Input D0 Negative Terminal |
| 60 | GND | Ground (0V) |
| 61 | RUN_PG | Bidirectional pin. Can be pulled low via a 220Ω resistor to achieve CM0 CPU reset; when functioning as an output, a high level indicates normal power status and CPU operation. Internally pulled up to CM0_3.3V power supply via a 10KΩ resistor. |
| 62 | GLOBAL_EN | Input pin; pulling this pin low disconnects the CM0 internal power supply. Pulled up to the 5V power rail via a 10KΩ resistor. |
| 63 | GND | Ground (0V) |
| 64 | CM0_1.8V (Output) | 1.8V ±5% accuracy. Maximum output current per pin: 300mA. Total output must not exceed 600mA. When GLOBAL_EN is set low, power supply will be cut off |
| 65 | CM0_1.8V (Output) | 1.8V ±5% accuracy. Maximum output current per pin is 300mA, with total output not exceeding 600mA; when GLOBAL_EN is set low, power supply will be cut off |
| 66 | GND | Ground (0V) |
| 67 | 5V (Input) | 4.75V to 5.25V Main Power Input |
| 68 | 5V (Input) | 4.75V to 5.25V Main Power Input |
| 69 | GND | Ground (0V) |
| 70 | NC | Not connected |
| 71 | NC | Not connected |
| 72 | GND | Ground (0V) |
| 73 | GPIO21 | GPIO Interface: Supports 3.3V signal level by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 74 | GPIO20 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 75 | GND | Ground (0V) |
| **Pin** | **Signal** | **Description** |

| | | |
|---|---|---|
| 76 | GPIO26 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 77 | GPIO16 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 78 | GND | Ground (0V) |
| 79 | GPIO19 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply. |
| 80 | GPIO13 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 81 | GND | Ground (0V) |
| 82 | GPIO12 | GPIO Interface: Supports 3.3V signal level by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 83 | GPIO6 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 84 | GND | Ground (0V) |
| 85 | GPIO5 | GPIO Interface: Supports 3.3V signal level by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 86 | ID_SC | (RP1 GPIO 1) GPIO: Typically operates at 3.3V signal levels, but can be configured for 1.8V signal levels by connecting GPIO_VREF to the CM0_1.8V power rail |
| 87 | GND | Ground (0V) |
| 88 | ID_SD | (RP1 GPIO 0) GPIO: Typically operates at 3.3V signal level, but can be configured for 1.8V signal level by connecting GPIO_VREF to the CM0_1.8V power rail |
| 89 | GPIO7 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply. |
| 90 | GND | Ground (0V) |
| 91 | GPIO8 | GPIO Interface: Supports 3.3V signal level by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 92 | GPIO11 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 93 | GND | Ground (0V) |
| 94 | GPIO25 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply, it can be switched to 1.8V signal mode |
| **Pin** | **Signal** | **Description** |

| | | |
|---|---|---|
| 95 | GPIO9 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 96 | GND | Ground (0V) |
| 97 | GPIO10 | GPIO Interface: Supports 3.3V signal level by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 98 | GPIO24 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 99 | GND | Ground (0V) |
| 100 | GND | Ground (0V) |
| 101 | GPIO23 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 102 | GPIO22 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 103 | GND | Ground (0V) |
| 104 | GPIO27 | GPIO Interface: Supports 3.3V signal level by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 105 | GPIO18 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 106 | GND | Ground (0V) |
| 107 | GPIO17 | GPIO Interface: Supports 3.3V signal level by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 108 | GPIO15 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 109 | GND | Ground (0V) |
| 110 | GPIO14 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 111 | GPIO4 | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply. |
| 112 | GND | Ground (0V) |
| 113 | GPIO3 | GPIO Interface: Supports 3.3V signal level by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply |
| 114 | GPIO2 | |
| **Pin** | **Signal** | **Description** |

| | | |
|---|---|---|
| | | GPIO Interface: Supports 3.3V signal levels by default, but can be switched to 1.8V signal mode by connecting the GPIO_VREF pin to the CM0_1.8V power supply.<br>CM0_1.8V power supply |
| 115 | GND | Ground (0V) |
| 116 | WiFi_ON | (This pin) may be left floating; if pulled low, the Wi-Fi interface will be disabled. Internally pulled up to CM0_3.3V power supply via a 10kΩ resistor |
| 117 | BT_ON | (This pin) may be left floating; if pulled low, the Bluetooth interface will be disabled. Internally pulled up via a<br>10kΩ resistor to CM0_3.3V power supply |
| 118 | LED_nACT | Low-active Raspberry Pi activity indicator; maximum drive current 5mA; this signal is typically used to drive the Active status indicator |
| 119 | CM0_3.3V (Output) | 3.3V ±5% accuracy. Maximum output current per pin is 300mA, with a combined total not exceeding 600mA; when<br>GLOBAL_EN is set low, power supply is cut off |
| 120 | CM0_3.3V (Output) | 3.3V ±5% accuracy. Maximum output current per pin: 300mA. Total output current must not exceed 600mA. When<br>GLOBAL_EN is set low, power supply will be cut off |
| 121 | RPI_BOOT | Setting this pin low forces boot from an RPI server (e.g., PC or Raspberry Pi). Leave floating if not using this feature. Internally pulled up to CM0_3.3V supply via 10kΩ resistor |
| 122 | SD_VREF | Must be connected to CM0_3.3V (Pins 119 and 120) to support 3.3V-level SD_CLK, SD_CMD, and SD_DAT0-3 signals; or connected to CM0_1.8V (Pins 64 and 65) to support corresponding 1.8V-level signals. This pin must not be left floating or grounded. |
| 123 | GND | Ground (0V) |
| 124 | SD_DAT1 | SD Card/eMMC Data1 Signal (Supported only by CM0Lite module) |
| 125 | SD_DAT0 | SD Card/eMMC Data0 Signal (Supported only by CM0Lite modules) |
| 126 | GND | Ground (0V) |
| 127 | SD_CLK | SD card clock signal (Supported only by CM0Lite module) |
| 128 | SD_CMD | SD card/eMMC command signal (Supported only by CM0Lite modules) |
| 129 | GND | Ground (0V) |
| 130 | SD_DAT3 | SD Card/eMMC Data3 Signal (Supported only by CM0Lite module) |
| 131 | SD_DAT2 | SD Card/eMMC Data2 Signal (Supported only by CM0Lite modules) |
| 132 | GND | Ground (0V) |

### 4.2.1 Pin Design Guidelines

The following guidelines provide grounding specifications, connector usage, voltage limits, power rail considerations, and precautions to prevent erroneous voltage application:

- Grounding Specifications: All ground pins must be connected.
- GPIO Voltage Limitations: Pins GPIO 0 through 27 adhere to the same specifications as the Pi5 40-Pin Connector. Voltage levels must not exceed the following signal level standards:
  - When using 3.3V: Must not exceed CM0_3.3V (Pins 119-120)
  - When using the 1.8V level: Must not exceed CM0_1.8V (Pins 64-65)
- Power Rail Usage Specifications: If the CM0_3.3V or CM0_1.8V power rail is used to supply devices other than the GPIO reference voltage (GPIO_VREF), an unexpected power loss protection mechanism must be designed (e.g., when the 5V line voltage drops below 4.5V):
  - When using the 1.8V power rail (CM0_1.8V): Ensure current drops to zero during power sags (no-load state)
  - When using the 3.3V power rail (CM0_3.3V): Ensure the 3.3V rail voltage remains higher than the 1.8V rail voltage at all times. Although 3.3V typically holds a higher level during power loss, design verification is still required. If 3.3V could potentially drop below 1.8V, implement circuitry to disconnect 3.3V devices to prevent damage.
- Reverse Voltage Protection: Do not apply reverse voltage to any pin. This means that when CM0 is powered down or shut off, no external voltage should be applied to any pin, as this may prevent CM0 from restarting.

### 4.2.2 Differential pairs

The length mismatch between positive (P) and negative (N) signal lines within a differential pair should be controlled within 0.15mm. The matching tolerance between different differential pairs may be appropriately relaxed based on interface type. For example, HDMI differential pairs typically allow a 25mm deviation, so standard circuit boards do not require additional matching processing.

- 100Ω Differential Pair Signal Length

All 100Ω differential pairs in CM0 have P/N signal length matching errors less than 0.1mm. Matching processing is also recommended for differential pairs on interface boards. Since most interfaces do not require precise matching between different differential pairs, CM0 does not fully maintain length consistency between differential pairs.

- 90Ω Differential Pair Signal Length

All 90Ω differential pairs (USB differential pairs) in CM0 have P/N signal length matching errors less than 0.1mm.

## 4.3 Electrical Specifications

To ensure safe and reliable operation of CM0, strictly adhere to the following electrical parameters and limitations.

### 4.3.1 Absolute Maximum Ratings

> Warning
>
> Exceeding the values listed in Table 6 may cause permanent damage to the device. These ratings are stress reference values only and do not imply that the device will operate normally under any conditions outside the ranges specified in the operating section. Prolonged exposure to absolute maximum ratings may affect device reliability.

Table 6 lists the absolute maximum ratings for critical voltage parameters of CM0. These values represent critical limits that may cause equipment damage; exceeding these limits is strictly prohibited.

Table 6 Absolute Maximum Ratings

| Name | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| VIN | 5V input voltage | -0.5 | 6.0 | V |
| VGPIO_VREF | GPIO voltage | -0.5 | 3.6 | V |
| Vgpio | GPIO Input Voltage | -0.5 | $V_{GPIO\_VREF}$ + 0.5 | V |

Note

$V_{GPIO\_VREF}$ is the GPIO group reference voltage and must be connected to the CM0_3.3V or CM0_1.8V power rail.

## 4.3.2 DC Electrical Characteristics

Table 7 details the DC electrical parameters for CM0 GPIO pins. This table describes the performance characteristics of GPIO pins under various conditions (e.g., different reference voltages) and provides the expected ranges for each parameter (minimum, typical, and maximum values).

Table 7 DC Electrical Characteristics

| Name | Parameter | Condition | Minimum | Typical Value | Maximum | Unit |
|---|---|---|---|---|---|---|
| VIL(gpio) | Input Low Voltage | $V_{GPIO\_VREF}$ = 3.3V | 0 | - | 0.8 | V |
| VIH(gpio) | Input High Voltage | $V_{GPIO\_VREF}$ = 3.3V | 2.0 | - | $V_{GPIO\_VREF}$ | V |
| VIL(gpio) | Input Low Voltage | $V_{GPIO\_VREF}$ = 1.8V | 0 | - | $0.35*V_{GPIO\_VREF}$ | V |
| VIH(gpio) | Input High Voltage | $V_{GPIO\_VREF}$ = 1.8V | $0.65*V_{GPIO\_VREF}$ | - | $V_{GPIO\_VREF}$ | V |
| IIL(gpio) | Input leakage current | $V_{GPIO\_VREF}$ = 3.3V | - | - | 5 | μA |
| IIL(gpio) | Input leakage current | $V_{GPIO\_VREF}$ = 1.8V | - | - | 5 | μA |
| VOL(gpio) | Output Low Voltage | - | - | - | 0.4 | V |
| VOH(gpio) | Output High Voltage | $V_{GPIO\_VREF}$ = 3.3V | $V_{GPIO\_VREF}$ - 0.4 | - | - | V |
| VOH(gpio) | Output High Voltage | $V_{GPIO\_VREF}$ = 1.8V | $V_{GPIO\_VREF}$ - 0.4 | - | - | V |
| IOL(gpio) | Outputs low current | 16mA, $V_{GPIO\_VREF}$ = 3.3V | 18 | - | - | mA |
| IOH (GPIO) | High-Current Output | 16mA, $V_{GPIO\_VREF}$ = 3.3V | 17 | - | - | mA |
| IOL(gpio) | Output Low Current | 16mA, $V_{GPIO\_VREF}$ = 1.8V | 12 | - | - | mA |
| IOH(gpio) | High-Current Output | 16mA, $V_{GPIO\_VREF}$ = 1.8V | 10 | - | - | mA |

| Name | Parameters | Condition | Minimum | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|---|
| RPU (GPIO) | Pull-up resistor | | 50 | - | 65 | kΩ |
| RPD(gpio) | Pull-down resistor | | 50 | - | 65 | kΩ |

### 4.3.3 Current Consumption

Table 8 lists the key current consumption characteristics of the CM0 under various operating conditions. This table details the typical shutdown current, idle current, and operating current measured at different input voltages and control signals. Actual values are closely related to the final application.

Table 8 CM0 Current Consumption Characteristics

| Name | Parameter | Condition | Minimum | Typical Value | Maximum | Unit |
|---|---|---|---|---|---|---|
| Vshutdown | Shutdown Current | GLOBAL_EN < 0.4V | - | 0.5 | - | mA |
| Vidle | Idle Current | GLOBAL_EN > 2V | - | 250 | - | mA |
| Vload | Operating Current | GLOBAL_EN > 2V | - | 670 | - | mA |

## 4.4 Thermal Characteristics

The BCM2837 (https://www.raspberrypi.com/documentation/computers/processors.html#bcm2837) system-on-chip (SoC) used in the CM0 incorporates thermal management functionality. When the chip temperature approaches 85°C, it automatically reduces the clock frequency to control temperature. To prevent overheating, the SoC may automatically activate performance throttling mechanisms at high ambient temperatures. If temperature cannot be effectively controlled through throttling, the chip case temperature may exceed 85°C. Any thermal management solution must ensure other semiconductor components on the board operate within safe ambient temperature limits.

The CM0's overall operating temperature range is -20°C to +85°C (non-condensing environment). Wireless RF performance is optimized within the -20°C to +75°C temperature range.

## 4.5 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) measures the average expected operational duration before a device fails. Table 9 displays the MTBF values for CM0 under various environmental conditions (these values vary with environmental conditions).

> Note
>
> The MTBF times shown in Table 9 do not include the CM0Lite.

Table 9 MTBF Values for CM0

| Environment | Description | CM0 MTBF |
|---|---|---|
| Ground Controlled Environment | | 374,000 hours |
| Environment | Description | CM0 MTBF |

| | | |
|---|---|---|
| | A stable, fixed controlled environment where temperature and humidity are regulated, such as laboratories, commercial and research computer centers, medical equipment rooms, etc. Equipment typically has a longer lifespan in such environments. | |
| Ground Mobile Environment | High-stress environments are characterized by vibration, temperature fluctuations, humidity changes, and frequent movement, such as those encountered by vehicle-mounted equipment and handheld communication devices. In such environments, equipment lifespan is significantly reduced. | 32,000 hours |

# 5 Troubleshooting

The CM0 requires a stable power supply to initiate operation. It undergoes multiple power-up and startup phases before commencing operation. If an error occurs during any phase, the CM0 may fail to start or operate correctly. The following steps assist in diagnosing and resolving issues by examining hardware power supply voltages and signal load behavior:

1. Load Test 5V Power Supply: Pull the GLOBAL_EN signal low and apply a 0.5A external load to the 5V power supply. The voltage should remain above 4.75V (including noise), ideally exceeding 4.9V.
2. Verify GLOBAL_EN is High: Remove the GLOBAL_EN pull-down resistor, then confirm GLOBAL_EN transitions to a high logic level by measuring the pin voltage or checking its logic state.
3. Verify proper rise of each power rail voltage:
   - Check if the 3.3V supply rises above 3.15V. If not, the 3.3V supply is overloaded.
   - Check if the 1.8V supply rises above 1.71V. If not, the 1.8V supply is overloaded.
4. Verify RUN_PG is high: Measure the pin voltage to confirm it exceeds 3.15V.
5. Verify the boot process via the activity LED (LED_nACT): The LED should flash to indicate booting; check that it does not flash error codes. For interpreting error code patterns, refer to the Raspberry Pi official documentation on LED flashing codes (https://www.raspberrypi.com/documentation/computers/configuration.html#led-warning-flash-codes )

.

Additionally, we recommend avoiding known issues by ensuring your system software (firmware and kernel) is up to date. Newer versions include system improvements, and new kernel releases typically incorporate critical security patches and performance enhancements. Keeping your firmware updated resolves many system issues and improves stability.

# 6 Ordering Information

The CM0 is available in multiple models differentiated by wireless capabilities and eMMC storage capacity. Each CM0 model corresponds to a unique order code (part number) for identification.

## 6.1 Order Quantity and Packaging

You may order specific quantities of CM0 devices as needed: choose individual boxed shipments (each device packaged separately) or bulk orders (shipped consolidated in a single shipping carton). Small-batch products in individual paper boxes feature built-in ESD-coated protection, eliminating the need for additional antistatic bags. This packaging material is recyclable, contributing to waste reduction.

## 6.2 Part Numbering

Table 10 details the structure of CM0 ordering codes, specifying different options for modules, wireless capabilities, RAM specifications, and eMMC storage.

Table 10 CM0 Part Numbering Information

| Model | Wireless | RAM LPDDR2 | eMMC storage |
|---|---|---|---|
| CM0 | 0 = No | 00 = 512MB | 000 = 0GB (Lite) |
| | | | 008 = 8GB |
| | | | 016 = 16GB |
| | 1 = Yes | 00 = 512MB | 000 = 0GB (Lite) |
| | | | 008 = 8GB |
| | | | 016 = 16GB |
| **Example Model** | | | |
| CM0 | 1 | 00 | 016 |

## 6.3 Product Model

Table 11 lists available CM0 models by part number, detailing wireless support, RAM size, eMMC storage capacity, and RPL number. Other configurations are available upon custom order.

Table 11 CM0 Product Models (Including CM0Lite)

| Model | Wireless | RAM LPDDR2 | eMMC Storage | RPL Code |
|---|---|---|---|---|
| CM0000000 | - | 512MB | Lite (0 GB) | SC2230 |
| CM0000008 | - | 512MB | 8 GB | SC2231 |
| CM0000016 | - | 512MB | 16 GB | SC2232 |
| CM0100000 | Yes | 512MB | Lite (0 GB) | SC2233 |
| CM0100008 | Yes | 512MB | 8 GB | SC2234 |
| CM0100016 | Yes | 512MB | 16 GB | SC2235 |

# Raspberry Pi Compute Module Zero Development Board

## Documentation

The Raspberry Pi Compute Module Zero Development Board is an official Raspberry Pi product. The product brand belongs to Raspberry Pi, and the product IP belongs to Raspberry Pi.

This document is translated by Shanghai Jingheng Electronics Technology Co., Ltd. Due to limitations in translation capabilities, inaccuracies may occur. If you encounter incomplete or inaccurate content in the translated material, please contact us promptly at mailto: support@edatec.cn .

The final interpretation and most accurate documentation version shall be based on the official content released by Raspberry Pi.

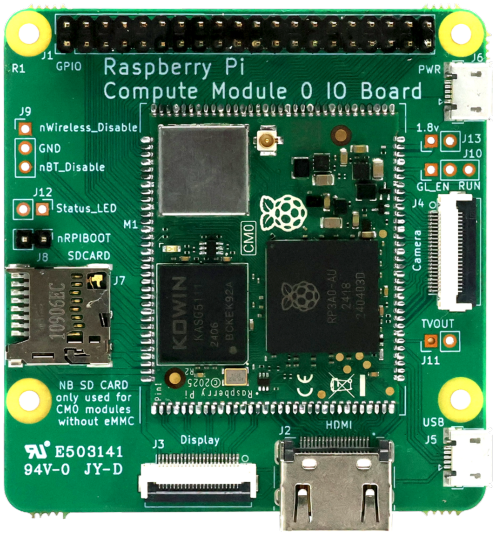
# 1 Introduction

This document introduces the definition and features of the Raspberry Pi Compute Module Zero Development Board (CM0 Dev Board).

## 1.1 Overview

The CM0 Dev Board is specifically designed for low-cost embedded prototyping, providing a complete CM0 development platform. This development board includes one Raspberry Pi CM0 (CM0), one Raspberry Pi CM0 IO Board (CM0IO Board), and one FPC antenna.

- Raspberry Pi CM0 (512MB SDRAM, 8GB eMMC, Wi-Fi/Bluetooth)
- Raspberry Pi CM0 IO Board
- FPC Antenna (3.5 dBi)




Note

The CM0 is pre-installed on the CM0IO board by default, and all references to the CM0IO board below include the CM0.

## 1.2 Features

Key features of the CM0 Dev Board include:

- 1GHz quad-core 64-bit Arm Cortex-A53 processor
- 512MB SDRAM, 8GB eMMC
- H.264/MPEG-4 video decoding (1080p@30fps); H.264 encoding (1080p@30fps)
- OpenGL ES 1.1/2.0 graphics processing standard
- 2.4GHz band 802.11 b/g/n wireless LAN
- Bluetooth 5.0 standard, supports Bluetooth Low Energy (BLE)
- 1 x FPC antenna, supports connection to CM0 via IPEX socket
- 1 x HDMI port supporting 1080p30Hz
- 1 x Micro USB port (J5), USB 2.0 interface
- 1 x Micro USB port (J6), power input interface
- 1 x MIPI DSI display port
- 1 x MIPI CSI camera interface
- 1 x Standard Raspberry Pi 40-Pin Header
- 1 x 2-Pin nRPIBOOT header
- Low-power design
- Reserved pins for LED, TVOUT, nBT_Disable, and nWireless_Disable
- Open-source hardware design

> Note
>
> The Bluetooth version of the CM0 in the initial small-batch trial production is Bluetooth 4.2. The Bluetooth version of the CM0 in the subsequent mass production batches is Bluetooth 5.0

# 2 CM0IO Specifications

This section details all interfaces, physical dimensions, and schematics included on the CM0IO board.

## 2.1 CM0IO Board Interfaces

This section details all interfaces included on the CM0IO board.

### 2.1.1 HDMI

The CM0IO board features one standard Type-A HDMI port compliant with the HDMI 1.3a standard. It supports resolutions up to 1080p at 30Hz and enables connection to HDMI displays.

### 2.1.2 DSI (MIPI Display)

The CM0IO board includes one MIPI DSI interface, a 22-pin 0.5mm pitch FPC connector, supporting connection to a Raspberry Pi Display via a 22-pin FPC cable.

> Note
>
> After connecting the Raspberry Pi Display, relevant configuration is required for normal operation.

### 2.1.3 CSI (MIPI Camera)

The CM0IO board features one MIPI CSI interface with a 22-pin, 0.5mm pitch FPC connector, supporting connection to the Raspberry Pi Camera via a 22-pin FPC cable.

> Note
>
> After connecting the Raspberry Pi Camera, relevant configuration is required for normal operation.

### 2.1.4 Micro-USB (Data)

The CM0IO board includes one Micro-USB (data) port, located at J5 on the board. It is compatible with the USB 2.0 standard and supports connecting standard USB 2.0 peripherals, with a maximum transfer rate of 480Mbps.

Disconnect power from the CM0IO board, short the 2-pin connector on nRPIBOOT (J8), then connect to a PC via this port. This will enter the CM0 into programming mode for eMMC programming.

### 2.1.5 Micro-USB (Power)

The CM0IO board includes one Micro-USB (Power) port, located at J6 on the board. It supports an external 5V power adapter to supply power to the CM0IO board.

### 2.1.6 Micro SD Card Slot

The CM0IO board includes one Micro SD card slot. However, since the Micro SD card slot is only applicable to the CM0 Lite, and the CM0 Dev Board comes standard with an 8GB eMMC, the Micro SD card slot is an inactive interface on the CM0 Dev Board.

### 2.1.7 nRPIBOOT Pin Header

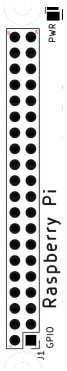
The CM0IO board includes one 2-pin nRPIBOOT header, located as J8 on the board, with pin definitions as nRPIBOOT/GND.

- Shorting nRPIBOOT and GND with a jumper cap: Powering the CM0 on again will enter programming mode.
- Unshort: Normal operating mode

### 2.1.8 Raspberry Pi 40-Pin Header

The CM0IO board includes one standard Raspberry Pi 40-pin interface, located on the board as J1. The specific pin definitions are listed in the table below.

| | Pin ID | Pin Name | Pin ID | Pin Name |
|---|---|---|---|---|




| | | | |
|---|---|---|---|
| 1 | +3.3V | 2 | +5V |
| 3 | GPIO2 | 4 | +5V |
| 5 | GPIO3 | 6 | GND |
| 7 | GPIO4 | 8 | GPIO14 |
| 9 | GND | 10 | GPIO15 |
| 11 | GPIO17 | 12 | GPIO18 |
| 13 | GPIO27 | 14 | GND |
| 15 | GPIO22 | 16 | GPIO23 |
| 17 | +3.3V | 18 | GPIO24 |
| 19 | GPIO10 | 20 | GND |
| 21 | GPIO9 | 22 | GPIO25 |
| 23 | GPIO11 | 24 | GPIO8 |
| 25 | GND | 26 | GPIO7 |
| 27 | ID_SD | 28 | ID_SC |
| 29 | GPIO5 | 30 | GND |
| 31 | GPIO6 | 32 | GPIO12 |
| 33 | GPIO13 | 34 | GND |
| 35 | GPIO19 | 36 | GPIO16 |
| 37 | GPIO26 | 38 | GPIO20 |
| 39 | GND | 40 | GPIO21 |

### 2.1.9 Reserved Pins

The CM0IO board includes multiple available pins to support user-defined external expansion.

#### 2.1.9.1 Wi-Fi & BT Pins

The CM0IO board features a 3-pin Wi-Fi & BT connector (J9) with the following pin definitions: nWireless_Disable/GND/nBT_Disable. Functions are as follows:

- Short nWireless_Disable to GND: Disables Wi-Fi functionality
- Short nBT_Disable to GND: Disables Bluetooth functionality

#### 2.1.9.2 GLOBAL_EN & RUN_PG Pins

The CM0IO board includes a 3-pin GLOBAL_EN & RUN_PG connector located at J10 on the board. The pins are defined as GLOBAL_EN/GND/RUN_PG with the following functions:

- Short GLOBAL_EN to GND: Holding the short for over 1ms forces a CM0 power-down reset
- Shorting RUN_PG and GND: Resets CM0

#### 2.1.9.3 TV_OUT Pin

The CM0IO board includes a 2-pin TV_OUT connector located at J11 on the board. The pins are defined as TV_OUT/GND and support extended 1 composite video signal.

#### 2.1.9.4 Status_LED Pin

The CM0IO board includes a 2-pin Status_LED pin located at J12 on the board. The pin is defined as Status_LED/GND and supports expansion of the CM0 LED status query port.

#### 2.1.9.5 1.8V Power Pin

The CM0IO board includes a 2-pin 1.8V power supply pin located at J13 on the board. The pin is defined as 1.8V/GND and supports the expansion of one 1.8V power output.

### 2.1.10 Wireless

The CM0IO board has Wi-Fi and Bluetooth enabled by default. After installing the FPC antenna, these features will function normally.

- 2.4 GHz Band IEEE 802.11 b/g/n Wireless Local Area Network
- Bluetooth 5.0 standard (supports BLE low-power mode)

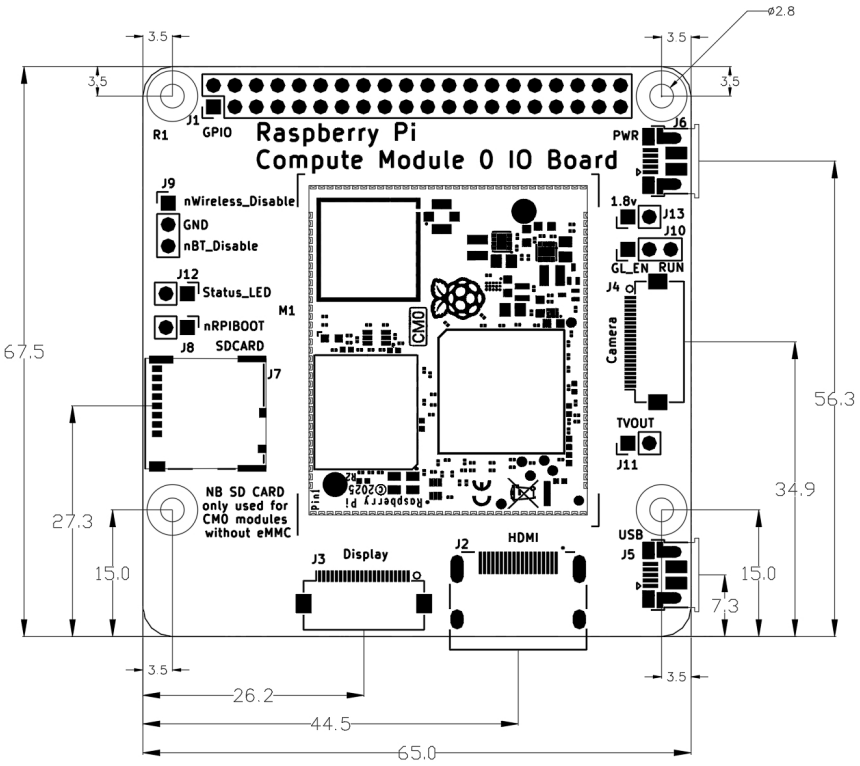
> Note
>
> The Bluetooth version for the initial small-batch trial production of CM0 is Bluetooth 4.2. The Bluetooth version for the later mass-produced CM0 units is Bluetooth 5.0

To disable Wi-Fi or Bluetooth, users can short-circuit the reserved pins on the CM0IO board.

- Short nWireless_Disable and GND: Disables Wi-Fi functionality
- Short nBT_Disable to GND: Disable Bluetooth functionality

## 2.2 CM0IO Board Dimensions

The CM0IO board measures 67.5 mm × 65 mm. Specific dimensions are shown in the figure below. Unit: mm

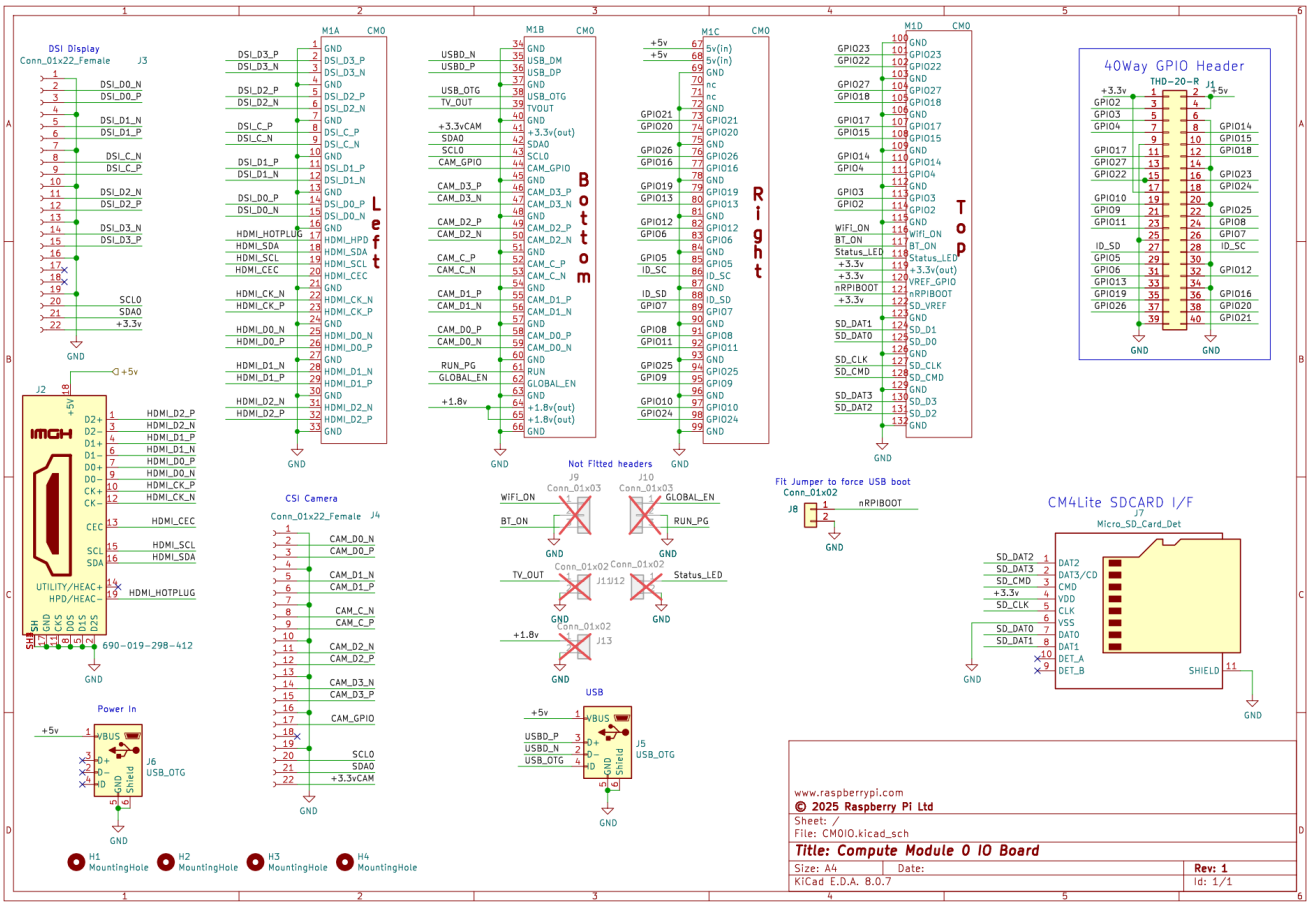



## 2.3 CM0IO Board Power Consumption

Power consumption of the CM0IO board under different states was tested, as detailed in the table below.

| Operating System | Test Conditions | Input Voltage | Input Current | Power Consumption |
|---|---|---|---|---|
| Raspberry Pi OS (Lite) 64-bit-bookworm | No Load | 4.97 V | 97.73 mA | 0.49 W |
| | Keyboard only | 4.97 V | 105.03 mA | 0.52 W |
| | Keyboard and HDMI connected | 4.96 V | 121.61 mA | 0.60 W |
| | Connect keyboard, HDMI, and Wi-Fi | 4.96 V | 146.84 mA | 0.73 W |
| | Connect keyboard, HDMI, and Wi-Fi, and add Wi-Fi stress test | 4.96 V | 282.93 mA | 1.40 W |
| | Connect keyboard, HDMI, and Wi-Fi, and add CPU stress test | 4.91 V | 369.99 mA | 1.82 W |
| | Connect keyboard, HDMI, and Wi-Fi, and add Wi-Fi stress test and CPU stress test | 4.90 V | 480.56 mA | 2.36 W |

## 2.4 CM0IO Board Schematic




# 3 FPC Antenna Specifications

Introduction to the specifications and physical dimensions of the FPC antenna.

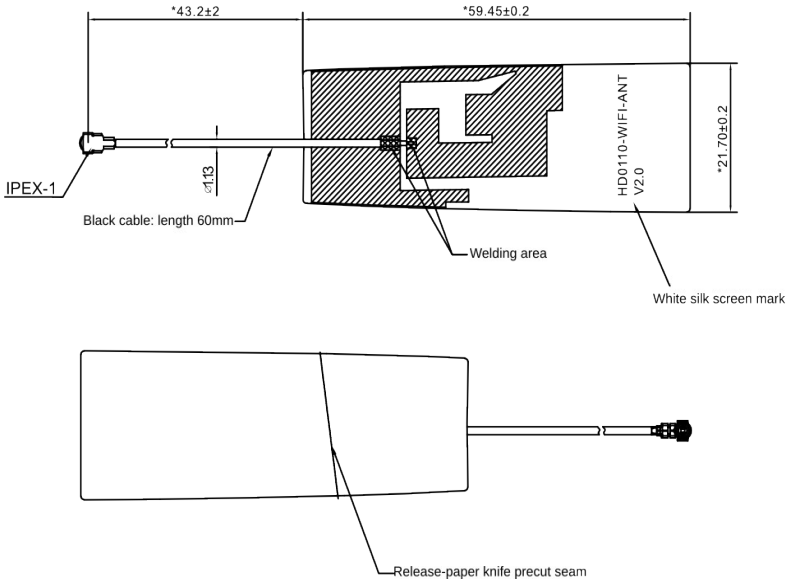
## 3.1 FPC Antenna Specifications

| Parameters | Specifications |
|---|---|
| Antenna Type | FPC + Cable |
| Operating Frequency Band (MHz) | 2400 ~ 2500, 5150 ~ 5850 |
| Gain (dBi) | 2450MHz: 3.5<br>5500MHz: 3.1 |
| Antenna Efficiency (%) | 2450MHz: 51.5<br>5500MHz: 43.5 |
| Voltage Standing Wave Ratio | ＜ 2.5:1 |
| Polarization | Linear Polarization |
| **Parameters** | **Specifications** |

| | |
|---|---|
| Radiation Pattern | Omnidirectional |
| Feed Impedance (ohms) | 50 |
| Power Capacity (dBm) | 33 |
| Antenna Interface | IPEX-1 |
| Antenna Dimensions (mm) | 59.45 x 21.7 |
| Weight (g) | 5 |
| Operating Temperature (°C) | -30° to 70° |
| Storage Temperature (°C) | -30°C to 70°C |

## 3.2 FPC Antenna Dimensions

Unit: mm




# 4 Ordering Code

| Model | Configuration |
|---|---|
| Raspberry Pi Compute Module Zero Development Board | Raspberry Pi CM0 (CM0100008, 512MB SDRAM, 8GB eMMC, Wi-Fi/BT) + Raspberry Pi CM0 IO Board + FPC Antenna |